



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/810,196	03/25/2004	Brian Holscher	TRAN-P247	8666
45590 7590 09/01/2009 TRANSMETA C/O MURABITO, HAO & BARNES LLP TWO NORTH MARKET STREET THIRD FLOOR SAN JOSE, CA 95113			EXAMINER GRU, SHAWN X	
			ART UNIT 2189	PAPER NUMBER
			MAIL DATE 09/01/2009	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/810,196

Applicant(s)

HOLSCHER ET AL.

Examiner

SHAWN X. GU

Art Unit

2189

Period for Reply -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 June 2009 and 20 July 2009.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-8508)
- 4) ☐ Interview Summary (PTO-413)
- 5) ☐ Notice of Individual Patent Application
- 6) ☐ Other: _____
- Paper No(s)/Mail Date _____

DETAILED ACTION

Response to Amendment

1. This Office action is in response to the claims and remarks filed 19 June 2009. Claims 1-24 are pending. All objections and rejections not repeated below are withdrawn.

Specification

2. The disclosure is objected to because of the following informalities:
On the cover sheet and first page of the specification, the title of the application should be amended to "Request Tracking Data Prefetcher Apparatus" to be consistent with the title of the invention.
Appropriate correction is required.

Claim Objections

3. Claims 18-20 and 22-24 are objected to containing the following minor informalities:
Per claim 18, on line 6, "the processor data requests" lacks sufficient antecedent basis and should be replaced by "processor data request".
Per claim 22, on lines 5-6, "the processor data requests" lacks sufficient antecedent basis and should be replaced by "processor data request".

All dependent claims are objected to for having the same deficiencies contained in the claims they are dependent from. Appropriate correction is required.

Claim Rejections - 35 USC § 101

4. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claims 1-8 and 22-24 rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. On page 13, lines 12-18 of the specification, the disclosure has provided evidence that the Applicant intended the apparatus in claim 1 to be a software program. Both the prefetcher and the tracker in claim 1 and the means in claim 22 appear to be implemented in software programs in at least one embodiment described in the disclosure. Computer programs not claimed as embodied in tangible media such as recordable media or computer storage media are descriptive material *per se* and are not statutory because they are not capable of causing functional change in the computer. They are neither computer components nor statutory processes, as they are not "acts" being performed. Such claimed computer programs do not define any structural and functional interrelationships between the computer program and other claimed elements of a computer which permit the computer program's functionality to be realized. Appropriate correction is required.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 1-16, 18, 21, 22 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Willke [US 6625696 B1] (hereinafter "Willke"), in further view of Ledeborn et al. [US 7,065,630 B1] (hereinafter "Ledeborn").

Independent Claims:

(A) Per claim 1, Willke teaches a request tracking data prefetch apparatus for a computer system, comprising:

a prefetcher (see col. 2, lines 48-67, storage controller 110 which comprises control logic 112) coupled to a high latency memory for a requesting device of the computer system (see col. 2, lines 21-47, Storage Device 120 which can be DRAM or other types of high latency memory for the requesting device 100, see col. 1, lines 20-29 and Fig. 3);

a tracker within the prefetcher and configured to recognize requesting device accesses to a plurality of cache lines within a low memory operable to supply data to the requesting device responsive to requesting device data requests, wherein the requesting device accesses form a stream type sequential access pattern, and wherein further the tracker is configured to use a bit vector to predictively load a target cache

line indicated by the stream-type sequential access pattern from the high latency memory into the low latency memory for the requesting device in preparation for the target cache line being requested by the requesting device as part of the stream-type requesting device access pattern (see col. 2, lines 48-67, col. 3, lines 1-25, col. 4, lines 48-51, col. 7, lines 29-40, note that the buffer 114 contains a set of stored access patterns and prediction and accuracy values for a requesting device 100, this set with the corresponding prefetching function in the storage controller 110 is construed to be a tracker; see col. 6, lines 41-67, col. 7, lines 1-28 and Fig. 3 for accesses to cache lines; see col. 3, lines 10-25, col. 7, lines 29-40 and col. 8, lines 30-35 for stream-type sequential access pattern; also see Fig. 5, items 510, 520, 540 and 560).

Willke does not specifically teach the requesting device is a processor except that the requesting device is a peripheral device (see Willke, col. 1, lines 8-9 and lines 46-50 and claim 12). Ledeböhm teaches a peripheral device in a computer system wherein the peripheral device is a graphics processor, see Ledeböhm, col. 4, lines 4-6 and Fig. 1). Ledeböhm's peripheral graphics processor provides a dedicated processing unit for the system's display device and provides functionalities such as generating pixels thereby freeing the main CPU from performing graphics control related tasks and increasing the overall performance of the computer system (see Ledeböhm, col. 4, lines 4-60). Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to including a graphics processor as one of Willke's peripheral requesting devices in order to provide dedicated display device control functionalities and to improve system performance. As a result of the

combined teaching of Willke and Ledebohm, the tracker within the prefetcher would be recognizing stream-type processor accesses and using a bit vector to prefetch cacheline data from adjacent addresses from a higher latency memory to a lower latency memory in anticipation of processor data requests. Also note that the high latency memory can be Ledebohm's graphics memory 116, Ledebohm's system memory 104, Willke's storage device 120, or a combination of these (see Ledebohm, col. 4, lines 47-67 and col. 6, lines 48-67, the graphics memory 116 is mapped to the virtual memory space).

(B) Per claim 9, Willke teaches a request tracking data prefetch apparatus for a computer system, comprising:

a requesting device (requesting device 100, see col. 1, lines 20-29 and Fig. 3);

a system memory (see col. 2, lines 21-47, Storage Device 120 which can be DRAM or other types of high latency memory) coupled to the requesting device;

a prefetch unit (see col. 2, lines 48-67, storage controller 110 which comprises control logic 112) coupled to the system memory;

a plurality of trackers included in the prefetch unit, wherein the trackers are respectively configured to recognize requesting device accesses to pages of the system memory (note that Willke teaches DRAM, see col. 2, lines 29-45), and configured to recognize accesses to cache lines within a cache memory operable to supply data to the requesting device responsive to requesting device data requests that form a stream type sequential access pattern; and

the cache memory coupled to the prefetch unit, wherein the prefetch unit uses a bit vector to predictively load target cache lines from the system memory into the cache memory to reduce an access latency of the requesting device in preparation for the target cache lines being requested by the requesting device as part the stream-type sequential requesting device access pattern, and wherein the target cache lines are indicated by the stream type sequential access pattern identified by the trackers (see col. 2, lines 48-67, col. 3, lines 1-25, col. 4, lines 48-51, col. 7, lines 29-40, note that the buffer 114 contains a set of stored access patterns and prediction and accuracy values for each requesting device, this set with the corresponding prefetching function in the storage controller 110 is construed to be a tracker; see col. 6, lines 41-67, col. 7, lines 1-28 and Fig. 3 for accesses to cache lines; see col. 3, lines 10-25, col. 7, lines 29-40 and col. 8, lines 30-35 for stream-type sequential access pattern; also see Fig. 5, items 510, 520, 540 and 560).

Willke does not specifically teach the requesting device is a processor except that the requesting device is a peripheral device (see Willke, col. 1, lines 8-9 and lines 46-50 and claim 12). Ledeborn teaches a peripheral device in a computer system

wherein the peripheral device is a graphics processor, see Ledebohm, col. 4, lines 4-6 and Fig. 1). Ledebohm's peripheral graphics processor provides a dedicated processing unit for the system's display device and provides functionalities such as generating pixels thereby freeing the main CPU from performing graphics control related tasks and increasing the overall performance of the computer system (see Ledebohm, col. 4, lines 4-60). Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to including a graphics processor as one of Willke's peripheral requesting devices in order to provide dedicated display device control functionalities and to improve system performance. As a result of the combined teaching of Willke and Ledebohm, the tracker within the prefetcher would be recognizing stream-type processor accesses and using a bit vector to prefetch cacheline data from adjacent addresses from a higher latency memory to a lower latency memory in anticipation of processor data requests. Also note that the high latency memory can be Ledebohm's graphics memory 116, Ledebohm's system memory 104, Willke's storage device 120, or a combination of these (see Ledebohm, col. 4, lines 47-67 and col. 6, lines 48-67, the graphics memory 116 is mapped to the virtual memory space).

(C) Per claims 18 and 22, it should be clear that the instant claim is already substantially described by claims 1 and 9 as set forth above. Note that Willke's buffer stores multiple stream-type access patterns for multiple requesting devices (see Willke, col. 4, lines 48-57 and col. 7, lines 29-40).

Dependent Claims:

(D) Per claims 2 and 10, Willke in view of Ledeböhm further teaches each of the trackers include a tag (see Willke, col. 2, lines 48-67, col. 3, lines 1-25, col. 4, lines 48-51, col. 7, lines 29-40; note that any configuration/setting data can be construed as a tag, and there are separate sets of prediction and accuracy values and stored access patterns for each processor) configured to recognize accesses to corresponding cache lines of the high latency memory by the processor (note that Willke teaches DRAM, see col. 2, lines 29-45, col. 6, line 52-67 and col. 7, lines 1-28).

(E) Per claims 3 and 11, Willke in view of Ledeböhm further teaches a plurality of system memory accesses by the processor to the high latency memory as recognized by the tag are used by the trackers to determine the target cache line for a predictive load into the cache memory/low latency memory (see Willke col. 2, lines 48-67, col. 3, lines 1-25, col. 4, lines 48-51, col. 7, lines 29-40 and the rejection of claims 1 and 9 set forth above; the stored access patterns are formed by multiple accesses by the corresponding requesting device; also note that both Willke's storage device 120 and/or Ledeböhm's graphics memory 116 can be viewed as a system memory because under the broadest reasonable interpretation a system memory is a memory associated as a system).

(F) Per claims 4, 12 and 24, Willke in view of Ledeböhm further teaches consecutive accesses by the processor to adjacent cache lines of a page of the system

memory are used to determine the target cache line of a stream type access pattern for a predictive load into the cache/low latency memory, wherein the adjacent cache lines have adjacent addresses, and wherein the target cache line is part of stream-type accesses that formed the stream-type access pattern (see Willke, col. 6, lines 41-67, col. 7, lines 1-28 and Fig. 3 for accesses to cache lines; see col. 3, lines 10-25, col. 7, lines 29-40 and col. 8, lines 30-35 for stream-type sequential access pattern and adjacent addresses).

(G) Per claim 5, Willke in view of Ledeborn further teaches the high latency memory comprises a memory block of a plurality of memory blocks of the computer system (see Willke, DRAM and disks, col. 2, lines 29-45, also see col. 6, line 52-67 and col. 7, lines 1-28; a memory block can be a cache line, a page, a byte, or any other unit of memory storage).

(H) Per claims 6 and 13, Willke does not specifically teach the system/high latency memory comprises a plurality of 4KB pages but teaches the high latency memory is a DRAM (see col. 2, lines 21-40). DRAM page sizes are determined by design choices and system specifications, and page sizes such as 4KB and 8KB are common in the art. Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to use 4KB as the page size in Willke's DRAM if dictated by design choice and system specification.

(I) Per claims 7 and 14, Willke in view of Ledeböhm further teaches each of the plurality of trackers includes a tag configured to monitor a sub portion of the high latency memory block/page for accesses by the processor (see Willke, col. 2, lines 48-67, col. 3, lines 1-25, col. 4, lines 48-51, col. 7, lines 29-40; note that any configuration/setting data can be construed as a tag, and there are separate sets of tracking/monitoring, prediction and accuracy values and stored access patterns for each requesting device; each of the stored access patterns only corresponds to a sub portion of the DRAM/the high latency memory).

(J) Per claim 8, Willke in view of Ledeböhm further teaches the high latency memory is a system memory of the computer system (see Willke, DRAM, col. 2, lines 29-45; also note that both Willke's storage device 120 and/or Ledeböhm's graphics memory 116 can be viewed as a system memory because under the broadest reasonable interpretation a system memory is a memory associated as a system).

(K) Per claim 15, Willke further teaches the cache line are 64 byte cache lines (see col. 7, lines 14-15) and a tag is used to monitor half of a page for accesses by the processor (here a page is broadly construed as an unit of storage that is twice the size of a cache line, also note that any configuration/setting data can be construed as a tag, and there are separate sets of prediction and accuracy values and stored access patterns for each requesting device, see the rejection of claim 2 set forth above), but does not teach the cache lines are 128 bytes. However, it is clear that cache line sizes are design dependent and it would have been obvious to one ordinarily skilled in the art

at the time of the Applicant's invention to make Willke's cache like size 128 bytes as a design choice.

(L) Per claim 16, Willke in view of Ledeböhm further teaches that the cache memory is a prefetch cache memory within the prefetch unit (see Willke, Fig. 1, Buffer 114 is within Storage Controller 110).

(M) Per claim 21, Willke in view of Ledeböhm further teaches said prefetch unit accesses to system memory are timed to utilize processor-to-system memory idle time (note that all memory accesses timed by a clock such as system clock in a digital computing system; also Willke, see col. 3, lines 10-25 and Fig.1 and 3, processor-to-system memory is idle during the time storage controller 110 accesses storage device 120 for prefetching and satisfying requesting device 100's requests, also storage controller 110 is only able to access storage device 120 when the processor/requesting device 100 is not directly accessing the storage device 120).

8. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Willke in view of Ledeböhm, further in view of Microsoft Computer Dictionary (hereinafter "Microsoft").

(N) Per claim 17, Willke in view of Ledeböhm does not specifically disclose that the cache memory is an L2 cache memory, but teaches the higher latency is a DRAM as set forth above in the rejection of claim 1. However, Microsoft discloses that a L2 cache is faster than DRAM and Willke's cache memory is a lower latency memory as compared to the higher latency DRAM. Therefore it would have been obvious to one

ordinarily skilled in the art at the time of the Applicant's invention to make Willke's cache memory a L2 cache because it is faster than DRAM.

9. Claims 19, 20 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Willke in view of Ledebohm, further in view of Brooks [6,081,868] (hereinafter "Brooks").

(O) Per claims 19 and 23, Willke in view of Ledebohm further teaches the computer system includes one main processor (see Willke, Fig. 4, CPU 400) and a peripheral graphics processor (Ledebohm's graphics processor), but does not specifically disclose that there are a plurality of main processors/CPU's and each of the CPU's is coupled to a respective high latency memory and a low latency memory. However, Brooks teaches a prefetch system wherein each of a plurality of CPU's is coupled to a respective high latency memory and a low latency memory (see Brooks: Fig 2, a CPU is coupled to a CPU private memory and a CPU cache in each CPU block; CPU Private Memory has higher latency than CPU Cache), in order to provide data storage exclusively for the associated CPU (Brooks: Col 5, Lines 25-30), higher performance and better fault tolerance. Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to increase the number of CPU's in Willke's invention and couple each of Willke's plurality of CPU's to a respective high latency memory and a low latency memory in order to provide increased performance and fault tolerance.

(P) Per claim 20, the claim recites substantially similar limitations as claims 4, 12 and 24 set forth above.

Response to Arguments

10. Applicant's arguments with respect to claims 1-24 have been considered but are moot in view of the new grounds of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Gu whose telephone number is (571) 272-0703. The examiner can normally be reached on 9am-5pm, Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Application/Control Number: 10/810,196

Page 15

Art Unit: 2189

/SHAWN X GU/

Shawn X Gu
Patent Examiner
Art Unit 2189

28 August 2009